Confirmation No. 6330

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appellant:	WAAYERS	Examiner:	Le, T.
Serial No.:	10/524,458	Group Art Unit:	2863
Filed:	February 10, 2005	Docket No.:	NL020749US
Title:	MODULE, ELECTRONIC DEVICE AND EVALUATION TOOL		

APPEAL BRIEF

Mail Stop Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Customer No.
65913

Dear Sir:

This Appeal Brief is submitted pursuant to 37 C.F.R. §41.37, in support of the Notice of Appeal filed October 25, 2007 and in response to the rejections of claims 1-12 as set forth in the Final Office Action dated April 26, 2007.

Please charge Deposit Account number 50-0996 (NXPS.365PA) $510.00 for filing this brief in support of an appeal as set forth in 37 C.F.R. §1.17(c). If necessary, authority is given to charge/credit Deposit Account 50-0996 additional fees/overages in support of this filing.

I. Real Party In Interest

The real party in interest is NXP Semiconductors. The application is presently assigned of record, at reel/frame nos. 016858/0396 to Koninklijke Philips Electronics, N.V., headquartered in Eindhoven, the Netherlands. We have been authorized by both the assignee of record and NXP Semiconductors to convey herein that the entire right, title and interest of the instant patent application have been transferred to NXP Semiconductors.

II. Related Appeals and Interferences

While Appellant is aware of other pending applications owned by the above-identified Assignee, Appellant is unaware of any related appeals, interferences or judicial proceedings that would have a bearing on the Board's decision in the instant appeal.

III. Status of Claims

Claims 1-3 and 11-12 stand rejected and are presented for appeal. Claims 4-10 have been indicated as containing allowable subject matter, and therefore are not presented for appeal. A complete listing of the claims under appeal is provided in an Appendix to this Brief.

IV. Status of Amendments

No amendments have been filed subsequent to the Amendment dated February 22, 2007. All of the claims on appeal, namely claims 1-3 and 11-12, are as originally presented.

V. Summary of Claimed Subject Matter

Appellant's application describes and claims a module that includes a functional block and a test controller for controlling the functional block in an evaluation mode. Appellant recognized that it can be desirable to freeze the content of a register to maintain a state of the associate module during a debug mode or evaluation mode. As such, Appellant's invention provides for blocking an update signal that otherwise would signal a responsive capturing of a bit pattern in a first register by a second register. Blocking the update can have the effect of freezing the contents of the second register.

In independent claim 1, Appellant recites a module (see, e.g., module 100 in Figs. 1-8, and accompanying text) that includes a functional block (see, e.g., functional block 120 in Figs. 1-8, and accompanying text) and a test controller (see, e.g., test controller 140 in Figs. 1-8, and accompanying text) for controlling the functional block in an evaluation mode of the module. Appellant further recites in claim 1 that the test controller includes a plurality of pins (see, e.g., dashed box around pins 162, 164, and 166 in Figs. 1-7, along with accompanying text) including an input pin (see, e.g., input pin 162 in Figs. 1-8, and accompanying text) and an output pin (see, e.g., output pin 164 in Figs. 1-8, and accompanying text), a first register (see, e.g., register 142 in Figs. 1-3, and accompanying text) coupled between the input pin and the output pin for receiving a bit pattern via the input pin and outputting the bit pattern via the output pin (see, e.g., paragraphs [0037] and [0038]); and a second register (see, e.g., register 144 in Figs. 1-3, and accompanying text) coupled to the first register for capturing the bit pattern responsive to an update signal (see, e.g., paragraph [0038]), and dedicated control circuitry (see, e.g., logic gates 180 and 182 shown in Figs. 1-3) for blocking the update signal responsive to the bit pattern (see, e.g., paragraph [0038]).

In independent claim 11, Appellants recite an electronic device (see, e.g., device 300 in Fig. 8, and accompanying text) that includes a plurality of modules (see, e.g., device 300 in Fig. 8, and accompanying text) being substantially serially interconnected in an evaluation mode through respective input pins and output pins (see, e.g., connections between pins 162 and 164 in Fig. 8, and accompanying text). Claim 11 further recites a module from the plurality of interconnected modules that is substantially similar to the module recited in claim 1.

VI. Grounds of Rejection to be Reviewed Upon Appeal

Claims 1-3 and 11-12 stand rejected under 35 U.S.C. 102(a) over "Testing and Programming Flash Memories on Assemblies During High Volume Production," by de Jong *et al.* (de Jong).

VII. Argument

A. The 102(A) Rejection Of Claims 1-3 And 11-12 Should Be Reversed Because De Jong Does Not Set Forth All The Elements Recited In Appellant's Claims.

A claim cannot be said to be anticipated by a reference unless that reference can be shown to set forth each and every element recited in the claim, including the recited arrangement. The Examiner has failed to make such a showing.

In supporting the rejection, the Examiner has generally cited to pages 477-478 of de Jong, including Figure 8 and Table 2. As set forth in the response dated February 22, 2007, Appellant has found nothing in the de Jong reference to teach or suggest a first register coupled between an input pin and an output pin (of a plurality of pins) for receiving a bit pattern via the input pin and outputting the bit pattern via the output pin, a second register coupled to the first register for capturing the bit pattern responsive to an update signal, and dedicated control circuitry for blocking the update signal responsive to the bit pattern. While de Jong appears to disclose more than one register component, the relationship of capturing a bit pattern in one register that is stored in another register in response to an update signal along with dedicated control circuitry for blocking the update signal are nowhere disclosed by de Jong.

The Examiner responded by quoting language from de Jong relating to "dedicated shift data registers" and "two unlock cycles," along with a conclusory statement that such disclosure amounts to dedicated control circuitry for blocking an update signal responsive to a bit pattern. The mere observation that de Jong may disclose dedicated shift data registers and multiple unlock cycles does not amount to a finding of correspondence between de Jong and the elements and relationships recited in Appellant's claims. Specifically, the Examiner has been unable to demonstrate that de Jong discloses capturing a bit pattern in a second register that is stored in a first register, and doing so in response to an update signal.

Furthermore, the Examiner has been unable to demonstrate that de Jong discloses dedicated control circuitry to block the update signal, thereby freezing the contents of the second register and the associated control signals.

At best, the Examiner has identified registers and unlock cycles in the de Jong reference, but has not correlated the relationships and functionality of the elements recited in Appellant's claims. An anticipation rejection cannot be predicated on mere identification of components in a reference that appear to correspond to individual elements recited in a claim. In electronics as well as in other fields, the relationships between and among the components must also be taken into account when evaluating the teachings of a reference against the claimed invention.

For at least these reasons, Appellant requests reversal of the rejection over de Jong.

B. The 102(A) Rejection Of Claims 1-3 And 11-12 Should Be Reversed As Improper For Failing To Provide Sufficient Detail.

To be in compliance with 35 U.S.C. § 132, sufficient detail must be provided by the Examiner regarding the alleged correspondence between the claimed invention and the cited reference to enable Applicant to adequately respond to the rejections. According to M.P.E.P. § 706.02(j), "[i]t is important for an examiner to properly communicate the basis for a rejection so that the issues can be identified early and the applicant can be given fair opportunity to reply." In this case, the Examiner has provided insufficient detail.

In the non-final Office Action mailed November 22, 2006, the Examiner cited to specific portions of de Jong that allegedly correspond to claim elements such as a plurality of pins and first and second registers. However, the Examiner failed to provide detailed support in de Jong for alleged disclosure of claimed aspects relating to relationships between the registers, the use of the update signal to affect the relationship between registers, and dedicated control circuitry for blocking the update signal. Instead, the Examiner pointed to general passages without setting forth specific correspondence.

Appellant sought additional guidance from the Examiner when stating in the response of February 22, 2007, "...there is no evident structure in Figure 8 or Figure 9 of de Jong to perform the function of blocking the update signal responsive to the bit pattern, as claimed."

As discussed in part A above, the Examiner responded by citing to the same passages of de Jong without providing any additional detail or specificity. Without providing further explanation for the basis of the Examiner's rejections, Appellant has not had fair opportunity to provide detailed response in reply to specific arguments, and has been forced to guess as to how the Examiner has been attempting to interpret the teachings of the de Jong reference.

For at least these reasons, Appellant requests that the rejection be reversed for failure to provide insufficient detail.

C. The Finality Of The 102(A) Rejection Of Claims 1-3 And 11-12 Should Be Withdrawn For Failure To Establish A Clear Issue Between Appellant And The Examiner.

According to M.P.E.P. § 706.07, "[b]efore final rejection is in order a clear issue should be developed between the examiner and applicant." Appellant submits that, due to the lack of specificity in alleging correspondence between the recited claims and the de Jong reference, a clear issue has not been developed between Appellant and the Examiner. In particular, the Examiner provided insufficient detail in the non-final Office Action mailed November 22, 2006, as discussed in part B above. For at least this reason, Appellant submits that the Office Action mailed April 26, 2007 was improperly made final.

VIII. Conclusion

In view of the above, Appellant submits that the rejections of claims 1-3 and 11-12 are improper. Appellant therefore requests reversal of the rejections as applied to the appealed claims and allowance of the entire application.

Authority to charge the undersigned's deposit account was provided on the first page of this brief.

Please direct all correspondence to:

Corporate Patent Counsel
NXP Intellectual Property & Standards
1109 McKay Drive; Mail Stop SJ41
San Jose, CA 95131

CUSTOMER NO. 65913

Respectfully Submitted,

By: _____
Name: Robert J. Crawford
Reg. No.: 32,122
Tel: 651 686-6633
(NXPS.356PA)

APPENDIX OF CLAIMS INVOLVED IN THE APPEAL
(S/N 10/524,458)

1. A module comprising a functional block and a test controller for controlling the functional block in an evaluation mode of the module, the test controller comprising:

a plurality of pins including an input pin and an output pin;

a first register coupled between the input pin and the output pin for receiving a bit pattern via the input pin and outputting the bit pattern via the output pin; and

a second register coupled to the first register for capturing the bit pattern responsive to an update signal;

characterized in that the test controller further comprises dedicated control circuitry for blocking the update signal responsive to the bit pattern.

2. A module as claimed in claim 1, characterized in that the dedicated control circuitry comprises a first logic gate having:

a first input for receiving the update signal;

a second input coupled to the first register for receiving the bit pattern; and

an output coupled to the second register.

3. A module as claimed in claim 2, characterized in that the dedicated control circuitry further comprises a plurality of logic gates coupled between the first register and the second input of the first logic gate for providing the second input with the bit pattern in a modified form.

11. An electronic device comprising a plurality of modules being substantially serially interconnected in an evaluation mode through respective input pins and output pins, a module from the plurality of interconnected modules comprising a functional block and a test controller for controlling the functional block in the evaluation mode of the module, the test controller comprising:

a plurality of pins including an input pin from the respective input pins and an output pin from the respective output pins;

a first register coupled between the input pin and the output pin for receiving a bit pattern via the input pin and outputting the bit pattern via the output pin; and a second register coupled to the first register for capturing the bit pattern responsive to an update signal;

characterized in that the test controller further comprises dedicated control circuitry for blocking the update signal responsive to the bit pattern.

12. An evaluation tool comprising a set of bit patterns for evaluating an electronic device as claimed in claim 11 by providing the electronic device with the set of bit patterns, characterized in that the set of bit patterns comprises a bit pattern for triggering the control circuitry to block the update signal responsive to the bit pattern.

APPENDIX OF CLAIMS NOT INVOLVED IN THE APPEAL
(S/N 10/524,458)

4. A module as claimed in claim 3, characterized in that the test controller further comprises:

a multiplexer having a control terminal, a first input, a second input, and an output coupled to the output pin;

a third register coupled between the input pin and the first input of the multiplexer; and

a no-update bypass register coupled between the input pin and the second input of the multiplexer;

the control terminal of the multiplexer being responsive to at least a part of the bit pattern.

5. A module as claimed in claim 4, characterized in that the dedicated control circuitry comprises a second logic gate having:

a first input coupled to the plurality of logic gates for receiving the bit pattern in the modified form;

a second input for receiving a further update signal; and

an output coupled to the third register, the third register being responsive to the further update signal.

6. A module as claimed in claim 4 or 5, characterized in that an output path of the plurality of logic gates comprises a data storage element responsive to the update signal for storing the bit pattern in the modified form.

7. A module as claimed in claim 2, characterized in that the test controller further comprises:

a further multiplexer having a first input, a second input, an output and a control terminal coupled to an output of the second register;

a first further register coupled between the input pin and the first input of the further multiplexer;

a second further register being responsive to the update signal, the second further register having at least an input coupled to the first further register; and a conductor coupled between the input pin and the second input of the further multiplexer;

the first register being coupled between the output of the multiplexer and the output pin; and

the second input of the first logic gate being coupled to the first register via the second register.

8. A module as claimed in claim 7, characterized in that the second further register is responsive to a reset signal.

9. A module as claimed in claim 7 or 8, characterized in that the second input of the first logic gate is coupled to the second register through a further logic gate, the further logic gate further being coupled to the first register.

10. A module as claimed in claim 7 or 8, characterized in that the dedicated control circuitry further comprises a plurality of logic gates being responsive to the bit pattern in the second register, the plurality of logic gates having their inputs coupled to the second further register and having at least an output coupled to the control terminal of the further multiplexer.

APPENDIX OF EVIDENCE

Appellant is unaware of any evidence submitted in this application pursuant to 37 C.F.R. §§ 1.130, 1.131, and 1.132.

APPENDIX OF RELATED PROCEEDINGS

As stated in Section II above, Appellant is unaware of any related appeals, interferences or judicial proceedings.